Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 14, with the following amended paragraph:

Self-timed semiconductor memories are well known in the art and are preferably used in high-speed applications. The read and write cycles in the self-timed memories are triggered by either the positive or the negative edge of a clock signal. The memory cycle continues until its completion, independent of the clock edge. Application of a duty cycle different than 50% has an effect on the detection of delay faults. A duty cycle smaller than 50% enables detection of delay faults causing slow-to-rise behavior in the memory address decoder. A duty cycle higher than 50% enables detection of delay faults causing slow-to-fall behavior in the memory address decoder. Furthermore, the clock duty cycle also stresses sense amplifiers, bit lines, pre-charge circuitry, and discharge circuitry, substantially increasing delay ~~faults~~ fault detection. It is known in the art that "at-speed" testing stresses the delay faults when the correct test patterns are implemented. However, implementation of a Built-In-Self-Test (BIST) for high frequency implies a substantial increase in area for the BIST, which is unacceptable for most applications. However, changing the duty cycle of the external clock has no effect on the detection of delay faults for self-timed semiconductor memories, because the positive or negative edge of the external clock does not control the end of the clock cycle. In self-timed memories termination of the read/write operation is determined internally depending on the dummy blocks. Therefore, it is not possible to control the sensitizing operation by increasing or reducing the duty cycle of the external clock making memory test a difficult task for detecting slow-to-rise and slow-to-fall delays.

Please replace the paragraph beginning on page 2, line 11, with the following amended paragraph:

In an embodiment according to the present invention, there is a method for providing an external clock signal to an internal memory block of a self-timed memory. The method comprises receiving an internal clock signal from a clock monitor of the self-timed memory, receiving an external clock signal, and receiving a control signal. The external clock signal has a duty cycle that is different from a duty cycle of the internal clock signal. In dependence upon the control signal, the internal clock signal is provided to the internal memory block during a normal mode of operation of the self-timed memory, and the external clock signal is provided to the internal memory block during a test mode of the self-timed memory ~~are provided~~.

Please replace the paragraph beginning on page 2, line 18, with the following amended paragraph:

In another embodiment according the present invention there is a self-timed memory that comprises an internal memory block. There is a clock monitor for receiving an external clock signal and for providing ~~an internal clock signal in dependence thereupon~~ a clock signal to the internal memory block. A test system is interposed between the clock monitor and the internal memory block. The test system comprises an internal clock signal input port in signal communication with the clock monitor for receiving ~~the~~ an internal clock signal, an external clock signal input port for receiving the external clock signal, a control signal input port for receiving a control signal, ~~an out put~~ and an output port in signal communication with the internal memory ~~block; and,~~ block. The test system also includes a multiplexer in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input ~~port~~ port, and the output port~~, the control circuitry~~ for receiving the internal clock signal, the external clock signal, and the control ~~signal, and for providing,~~ signal. The multiplexer also provides, in dependence upon the control signal, the internal clock signal via the output port to the internal memory block during a normal mode of operation of the self-

timed memory, and ~~for providing~~ the external clock signal to the internal memory block during a test mode of the self-timed memory.

Please replace the paragraph beginning on page 3, line 1, with the following amended paragraph:

In yet another embodiment according to the present invention there is a self-timed memory that comprises ~~at least~~ an internal memory block, a clock monitor for receiving an external clock signal and for providing ~~at least an internal clock signal in dependence thereupon~~ a clock signal to the ~~at least an~~ internal memory block, and a test system interposed between the clock monitor and the ~~at least an~~ internal memory block. The test system ~~comprises, at least~~ comprises an internal clock signal input port in signal communication with the clock monitor for receiving ~~at least an~~ the internal clock signal, an external clock signal input port for receiving the external clock signal, a control signal input port for receiving a control signal, ~~at least an out put~~ and an output port in signal communication with the ~~at least an~~ internal memory ~~block; and,~~ block. The test system also includes control circuitry in signal communication with the ~~at least an~~ internal clock signal input port, the external clock signal input port, the control signal input ~~port~~ port, and the ~~at least an~~ output port~~, the control circuitry~~ for receiving the ~~at least an~~ internal clock signal, the external clock signal, and the control ~~signal, and for providing,~~ signal. The control circuitry also provides, in dependence upon the control signal, the ~~at least an~~ internal clock signal via the ~~at least an~~ output port to the ~~at least an~~ internal memory block during a normal mode of operation of the self-timed memory, and ~~for providing~~ the external clock signal to ~~at least one of~~ the ~~at least an~~ internal memory block during a test mode of the self-timed memory.

Please replace the paragraph beginning on page 3, line 21, with the following amended paragraph:

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 (Prior Art) is a simplified block diagram schematically illustrating an address decoder with a clock monitor for generating an internal clock signal;

FIG. 2 is a simplified block diagram schematically illustrating the address decoder shown in FIG. 1 with a test system according to the invention;

FIGS. 3A-3C are simplified block diagrams schematically illustrating various embodiments of the test system according to the invention; and

FIG. 4 shows a detailed self-timed memory block diagram coupled with the test system according to an embodiment of the present invention; and

FIG. 5 is ~~flowchart~~ a flowchart of the steps in implementing an embodiment according to the present invention.

Please replace the paragraph beginning on page 4, line 23, with the following amended paragraph:

Referring to FIG. 1, a 2-to-4 address decoder 125 controlled by an internal clock signal PHIX is shown. Control ~~logic,~~ logic within a clock monitor 152 of the address decoder ~~150~~ 125 is initiated based on the positive or negative edge of an external clock signal CL. The control logic 152 then generates the internal clock signal PHIX. Word line activation and deactivation is controlled depending on the positive or negative edge of the internal clock signal PHIX. Hence, the activation and deactivation of the word lines is independent of the external clock signal CL. Therefore, the detection of slow-to-rise and slow-to-fall delay faults depends on the duty cycle of the internal clock signal PHIX and not the external clock signal CL. The chip select CS is a signal that activates an operation of the memory. In one example memory, when CS is a logic "1", the memory is activated for read or write ~~operation~~ operations. In other example memory,

when CS is a logic "0," the memory is ~~activate~~ activated for read or write ~~operation~~ operations. Consequently, depending upon the design of the memory, inv_2 (109) may be replaced with a buffer instead.

Please replace the paragraph beginning on page 5, line 3, with the following amended paragraph:

Referring to FIG. 2, a test system 100 according to the invention connected to the 2-to-4 address decoder 125 is shown. The test system 100 includes ~~a clock~~ clock signal input ports 104 and 106 for receiving the internal clock signal PHIX from the clock monitor 152 and the external clock signal CL, respectively. Depending on a control signal received at ~~control input port 108~~ a control input port 108, a multiplexer 110 provides via output port 102 the internal clock signal 107 (PHIX) or the external clock signal CL to the address decoder 125. Depending on the received control signal, the multiplexer 110 provides the internal clock signal PHIX to the address decoder 125 in normal mode or the external clock signal CL during test mode. Interposing the test system 100 between the clock monitor 152 and the address decoder 125 enables control of the clock cycle of the address decoder 125, by directly applying the external clock signal CL to the address decoder 125 during test mode. Thus, the beginning and the end of the activation and deactivation of the word lines is easily controlled by the external clock signal CL enabling the detection of delay faults. As is evident, the test system is easily extended to cover a plurality of internal memory blocks that are controlled by the internal memory clock such as sense amplifier, column and bank decoder, pre-charge and discharge circuitry, and input/output latches.

Please replace the paragraph beginning on page 5, line 24, with the following amended paragraph:

In the ~~implementation,~~ implementation shown in FIG. 3A, two test systems 100, 100 are interposed between the clock monitor 152 and each of the internal memory blocks 150 and 151, i.e. one test system is used for controlling one internal memory

block 150 and 151, respectively. A buffer 131 couples the clock monitor 152 to the inputs of test systems 100, 100'.

Please replace the paragraph beginning on page 5, line 28, with the following amended paragraph:

Alternatively, as shown in FIG. 3B, one test system 200 having two output ports 201 and 202, respectively, is interposed between the clock monitor 152 and the internal memory blocks 150 and 151. Depending on a control signal received at ~~control input port 208~~ a control input port 208, a multiplexer 210 provides via the output ports 201 and 202 the internal clock signal PHIX, received at input port 204, or the external clock signal CL, received at input port 206, to the internal memory blocks 150 and 151, respectively. Depending on the received control signal the test system 200 provides the internal clock signal PHIX to the internal memory blocks 150 and 151 in normal mode or the external clock signal CL during test mode. A buffer 231 couples one output of the clock monitor 152 to an input of the test system 200.

Please replace the paragraph beginning on page 6, line 4, with the following amended paragraph:

In the example ~~embodiment,~~ embodiment shown in FIG. 3C, the test system 300 receives via input ports 304 and 305 two internal clock signals for the internal memory blocks 150 and 151, respectively. Depending on a control signal received at ~~control input port 308~~ a control input port 308, a multiplexer 310 provides via output ports 301 and 302 the internal clock signals received at the input ports 304 and 305, or the external clock signal CL, received at input port 306, to the internal memory blocks 150 and 151, respectively. Buffers 331, 332 couple outputs of the clock monitor 152 with inputs 304, 305 of the test system 300.

Please replace the paragraph beginning on page 6, line 11, with the following amended paragraph:

Referring to ~~FIG. 4. A~~ FIG. 4, a test system 410 according to an embodiment of the present invention is coupled to a self-timed memory 415. The test system 410 generates the clock 430 for the address decoders and the internal clock 425 (PHIX) for controlling the other blocks of the memory 415. The test system 410 has a test mode input 411, input for ~~external~~ an external clock signal 412, and input for a chip select 413.